Patent

Docket No.: RESH-001

Information Disclosure Statem nt Transmittal

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner of Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.					
Date of Deposit:	11/03/03	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Peter Dahl, Byron Dickinson, Margie Levine and Paul Rodman

Serial No.: 09/714,722 Group Art Unit: 2811

Filed: 11/15/00 Examiner: TRAN, T.

Title: OPTIMIZATION OF ABUTTED-PIN HIERARCHICAL PHYSICAL DESIGN

Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450
Sir:

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

..... Formal drawings, totaling ..... sheets.
..... Informal drawings, totaling ..... sheets.
..... Certification for PTO Consideration
..... Information Disclosure statement (__ sheets)
..X.. Information Disclosure statement and late filing fee
..X.. Form 1449
..... Petition for Extension of Time
..X.. Other: REFERENCES

F Calculation (for other than a small entity)					
Fee Items				Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere				$ .00	$0.00
Information Disclosure Statement, late filing				$180.00	$180.00
Other:					$0.00
T tal Fees					$180.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085 .
A duplicate copy of this authorization is enclosed.

[X] A check in the amount of $180.00

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

11/13/2003 SZEWDIE1 00000045 09714722

01 FC:1806 180.00 OP

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 11/3/2003

By: Jose S. Garcia
Jose S. Garcia
Reg. No. 43,628

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: RESH-001

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Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
6,618,849	METHOD AND APPARATUS FOR IDENTIFYING ROUTES FOR NETS	0/9/09/03
5,576,969	IC COMPRISING FUNCTIONAL BLOCKS FOR WHICH A MASK PATTERN IS PATTERNED ACCORDING TO CONNECTION AND PLACEMENT DATA	11/19/96
6,243,854	METHOD FOR SELECTING HIERARCHICAL INTERACTIONS IN A HIER-ARCHICAL SHAPES PROCESSOR	06/05/01
5,544,088	METHOD OF I/O PIN ASSIGNMENT IN A HIERARCHICAL PACKAGING SYSTEM	08/06/96
5,533,148	METHOD FOR RESTRUCTURING PHYSICAL DESIGN IMAGES INTO HIER-ARCHICAL DATA MODELS	07/02/96
5,187,671	AUTOMATED INTERCONNECT ROUTING SYSTEM	02/16/93
4,890,238	METHOD FOR PHYSICAL VLSI-CHIP DESIGN	12/26/89

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Patent Application

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Serial No.: 09/714,722 Group Art Unit: 2811

Filed: 11/15/00 Examiner: TRAN, T.

Title: OPTIMIZATION OF ABUTTED-PIN HIERARCHICAL PHYSICAL DESIGN

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	6,618,849	09/09/03	Teig et al.	716	12	01/13/02
	B	6,243,854	06/05/01	Lavin et al.	716	19	04/28/98
	C	5,544,088	08/06/96	Aubertine et al.	364	489	06/19/95
	D	5,533,148	07/02/96	Sayah et al.	382	240	09/30/93
	E	5,187,671	02/16/93	Cobb	364	490	08/24/90
	F	4,890,238	12/26/89	Klein et al.	364	491	12/15/87
	G	5,576,969	11/19/96	Aoki et al.	364	491	03/09/94

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	H							
	I							
	J							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	K	

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.